

REMARKS

Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Claims 1, 7, 13, and 18-19 are amended. Claims 14-15 have been withdrawn from consideration. Claim 20 is newly added. Claims 16-17 are cancelled without prejudice or disclaimer. After entry of this amendment, claims 1-4, 6-11, 13-15, and 18-20 will remain pending in the application.

The drawings were objected to under 37 CFR 1.83(a). The objection to the drawings is respectfully traversed. Applicant respectfully submits that a plurality of MOSFETs disposed in comb-like shape on the semiconductor substrate is illustrated in FIG. 9 of the drawings. In this regard, the attention of the Examiner is directed to page 1, lines 12-37, of the specification which provides a detailed description of FIG. 9. This figure clearly shows a plurality of MOSFETs disposed in a comb-like shape. This plurality of MOSFETs includes a "plurality of gate electrodes" 7 and "contact holes" 9 (See p. 1, lines 15-24). Accordingly, reconsideration and withdrawal of the objection to the drawings are respectfully requested.

Claim 13 was objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. In response, the dependency of claim 13 has been changed from claim 1 to claim 7. Applicant respectfully submits that the amendment to claim 13 obviates the rejection. Accordingly, reconsideration and withdrawal of the objection to claim 13 are respectfully submitted.

Claims 7-11, 16-17 and 19 were rejected under 35 U.S.C. §112, second paragraph. The rejection is respectfully traversed.

The Office Action alleges that it is unclear whether the limitation "this layer" in line 13 is referring to the low resistance layer stated in line 12 or the polysilicon layer stated in line 10. In response, claim 7 has been amended to positively recite that the layer provided directly under the signal input pad and acting as a shield is the low resistance layer. Therefore, it is respectfully submitted that the amendment to claim 7 obviates the rejection.

The Office Action further alleges that it is unclear whether the gate of the MOSFET in line 4 is the same structure as the polysilicon layer provided beneath said signal input in line 10. The Office Action then contends that "it appears from the Applicant's disclosure (see FIGS. 6A and 6B wherein element 141 is identified as the gate polysilicon layer) that they are." Applicant respectfully disagrees with this statement and respectfully submits that the

gate element of the MOSFET and the polysilicon layer provided beneath the signal input pad are two different structures. In FIG. 6A, contrary to what is stated in the Office Action, the polysilicon layer is referenced with reference number 141 while the polysilicon gate is referenced with reference number 107. Therefore, it is respectfully submitted that the polysilicon layer and the polysilicon gate are clearly identified as being two separate structures. In addition, claim 7 clearly recites a semiconductor device comprising, *inter alia*, a signal input pad connected to a gate of the MOSFET and a polysilicon layer provided beneath said signal input pad. Therefore, it is respectfully submitted that, contrary to what is stated in the Office Action, claim 7 clearly recites two different structures: a gate and a polysilicon layer.

Claims 8-11 and 19 depend from claim 7 and are patentable for the same reasons given above related to claim 7.

Claims 16 and 17 have been cancelled without prejudice or disclaimer, thus rendering moot the rejection of claims 16 and 17.

Accordingly, reconsideration and withdrawal of the rejection of claims 7-11, 16-17 and 19 under 35 U.S.C. §112, second paragraph, are respectfully requested.

Claims 1-4, 16, and 18 were rejected under 35 U.S.C. §103(a) based on Jarstad et al. (U.S. Pat. No. 6,472,723) (Jarstad) in view of Iguchi et al. (U.S. Pat. No. 5,744,394) (Iguchi). The rejection is respectfully traversed.

Claim 16 has been cancelled without prejudice or disclaimer, thus rendering moot the rejection of claim 16.

With respect to claim 1, the Office Action concedes that Jarstad fails to disclose a low resistance layer provided on the upper surface of the high concentration impurity diffusion region and directly under the signal input pad. While Applicant agrees with this statement, it is respectfully submitted that claim 1 is also patentable over Jarstad at least because it recites a semiconductor device comprising, *inter alia*, a MOSFET formed on the substrate, a signal input pad connected to a gate of the MOSFET, said signal input pad receiving an input signal for the MOSFET, and a high concentration impurity diffused region located beneath the signal input pad and at a surface part of the semiconductor substrate, wherein the high concentration impurity diffused region is a substrate/well potential take-out region. (Emphasis added)

In contrast to the semiconductor device recited by claim 1, Jarstad recites a semiconductor component comprising a substrate 101 and a MOSFET having a gate,

source/drain areas and contacts 119. However, contrary to what is stated in the Office Action, the source/drain areas of Jarstad do not correspond to the high concentration region recited in claim 7. These areas merely correspond to the ordinary active regions of a MOS transistor and therefore are not part of the substrate/well potential take-out region of claim 7. In addition, it is respectfully submitted that Jarstad fails to teach or suggest a high concentration impurity diffused region located beneath the signal input pad connected to a gate of the MOSFET. In Jarstad, the element that takes-out the substrate potential is metal plug 205. However, it is respectfully submitted that this element is neither connected to any high-concentrated impurity diffusion region nor provided beneath the signal input pad.

It is respectfully submitted that Iguchi fails to overcome the deficiencies of Jarstad. Namely, Iguchi fails to teach or suggest, for example, a high concentration impurity diffused region located beneath the signal input pad and at a surface part of the semiconductor substrate, wherein the high concentration impurity diffused region is a substrate/well potential take-out region. Therefore, as none of the applied art teaches or suggests all the elements of claim 1, the combination of Jarstad with Iguchi would not result in the invention of claim 1.

Claims 3-4 and 18 are patentable by virtue of their dependency from claim 1 and for the additional features recited therein.

Accordingly, reconsideration and withdrawal of the rejection of claims 1-4, 16, and 18 under 35 U.S.C. §103(a) based on Jarstad in view of Iguchi are respectfully requested.

Claims 7-11, 17 and 19 were rejected under 35 U.S.C. §103(a) based on Jarstad in view of Iguchi as applied to claims 1-4, 16, and 18 above, and further in view of Hsu et al. (U.S. Pat. No. 5,241,203) (Hsu). The rejection is respectfully traversed.

Claim 17 has been cancelled without prejudice or disclaimer, thus rendering moot the rejection of claim 17.

With respect to claim 7, the Office Action concedes that Jarstad and Iguchi fail to disclose a polysilicon layer provided beneath the signal input pad. While Applicant agrees with this statement, it is respectfully submitted that claim 7 is also patentable over Jarstad and Iguchi for the same reasons provided above related to claim 1. Namely, claim 7 is also patentable over Jarstad and Iguchi at least because it recites a semiconductor device comprising, *inter alia*, a signal input pad connected to a gate of the MOSFET, said signal input pad receiving an input signal for the MOSFET, a high concentration impurity diffused region located below the signal input pad and at a surface part of the semiconductor substrate, and an interconnection connected to the high concentration impurity diffused region, said

interconnection being electrically isolated from said signal input pad, wherein the high concentration impurity diffused region is a substrate/well potential take-out region.

It is respectfully submitted that Hsu fails to overcome these deficiencies. In this regard, it should be noted that the heavily doped region 44B, which the Examiner is referring to in the Office Action, does not correspond to a substrate/well potential take-out region as recited in claim 7. Instead, this region corresponds to the source/drain areas of the transistor device. Therefore, as none of the applied art teaches or suggests all the elements in claim 7, the combination of Jarstad with Iguchi and Hsu would not result in the invention of claim 7.

Claims 8-11, and 19 are patentable by virtue of their dependency from claim 7 and for the additional features recited therein.

Accordingly, reconsideration and withdrawal of the rejection of claims 7-11, 17 and 19 under 35 U.S.C. §103(a) based on Jarstad in view of Iguchi as applied to claims 1-4, 16, and 18 above, and further in view of Hsu are respectfully requested.

Claims 6 and 13 were rejected under 35 U.S.C. §103(a) based on Jarstad in view of Iguchi as applied to claims 1-4, 16, and 18 above, and further in view of Battersby et al. (U.S. Pat. No. 5,528,065) (Battersby).

Claim 6 depends from claim 1 and is, therefore, patentable over Jarstad and Iguchi for at least the same reasons given above related to claim 1. Namely, it is respectfully submitted that claim 6 is patentable over Jarstad and Iguchi at least because it recites a semiconductor device comprising, *inter alia*, a MOSFET formed on the substrate, a signal input pad connected to a gate of the MOSFET, said signal input pad receiving an input signal for the MOSFET, and a high concentration impurity diffused region located beneath the signal input pad and at a surface part of the semiconductor substrate, wherein the high concentration impurity diffused region is a substrate/well potential take-out region.

It is respectfully submitted that Battersby fails to overcome these deficiencies. Therefore, as none of the applied art teaches or suggests all the elements of claim 6, the combination of Jarstad with Iguchi and Battersby would not result in the invention of claim 6.

Claim 13 depends from claim 7 and is, therefore, patentable over Jarstad and Iguchi at least for the same reasons given related to claim 7. Namely, it is respectfully submitted that claim 13 is patentable over Jarstad and Iguchi at least because it recites a semiconductor device comprising, *inter alia*, a signal input pad connected to a gate of the MOSFET, said signal input pad receiving an input signal for the MOSFET, a high concentration impurity diffused region located below the signal input pad and at a surface part of the semiconductor

substrate, and an interconnection connected to the high concentration impurity diffused region, said interconnection being electrically isolated from said signal input pad, wherein the high concentration impurity diffused region is a substrate/well potential take-out region.

It is respectfully submitted that Battersby fails to overcome these deficiencies. Therefore, as none of the applied art teaches or suggests all the elements of claim 13, the combination of Jarstad with Iguchi and Battersby would not result in the invention of claim 13.

Accordingly, reconsideration and withdrawal of the rejection of claims 6 and 13 under 35 U.S.C. §103(a) based on Jarstad in view of Iguchi as applied to claims 1-4, 16, and 18 above, and further in view of Battersby are respectfully requested.

Claim 20 is newly added. It is respectfully submitted that new claim 20 is supported by the specification. No new matter has been entered. Accordingly, it is respectfully submitted that claim 20 is in condition for allowance.

In view of the foregoing, the claims are now believed to be in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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